ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE YIELD AND RELIABILITY OF VLSI DESIGNS

Application Number : 10/604962 8/28/03

Confirmation Number:

First Named Applicant: Robert Allen

Attorney Docket Number: BUR920030092US1

Art Unit: 2825

Examiner: Siek, V.

Search string: (4831725 or 5459690 or 5796274 or 5798937 or 6026224 or 6189132 or 6484301 or 6556658).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
VS	1	4831725	1989-05-23	Dunham et al.			
	2	5459690	1995-10-17	Rieger et al.			
	3	5796274	1998-08-18	Willis et al.			
	4	5798937	1998-08-25	Bracha et al.			
	5	6026224	2000-02-15	Darden et al.			
	6	6189132	2001-02-13	Heng et al.			
	7	6484301	2002-11-19	Burden			
VS	8	6556658	2003-04-29	Brennan			

Signature

Examiner Name	Date
VUTHE SIEK	5/6/05